REMARKS

I. Introduction

Applicants note with appreciation the indication of allowance of claims 2, 3, 5, 8 and 11. In response to the Office Action mailed May 20, 2004, Applicants have amended claim 6 to further clarify the claimed subject matter. Support for this amendment can be found, for example, in Fig. 9 and its corresponding section of the specification. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claim 6 is rejected under 35 U.S.C. § 102 as being anticipated by USP No. 5,113,415 to Muto. Applicants respectfully traverse this rejection for at least the following reasons.

As recited by claim 6, the present invention relates to a digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form, wherein a differential value of synchronous signals of reception packet data, which should be of the same level by nature, is determined so as to detect a clock phase error of transmission data, and a clock signal is regenerated by phase control on the basis of said clock phase error, said digital broadcast demodulator further comprising a subtracting circuit for subtracting the N-th input from the N+1th input of all reception data, a circuit for outputting the subtraction input value obtained in step (a) only for the data coinciding

with the code pattern of segment synchronous signal, and a circuit for outputting said subtraction input value obtained in step (b) as a clock phase error signal only for the data positioned at the segment synchronous signal, wherein only the phase errors of the second symbol and the third symbol of the segment synchronous signal are outputted as said clock phase error.

More specifically, in accordance with one embodiment of the present invention, the digital data output from the A/D converter 12 is fed into the addition input of an subtracting circuit 202 through a latch 203. The digital data is further fed into the subtraction input of the subtracting circuit 202 through a latch 204. In the subtracting circuit 202, the N-th input is subtracted from the N+1-th input, and the resulting value is then fed into a latch circuit 207. In the latch circuit 207, the data is latched by the signal "Sdet" of the code pattern detection of the segment synchronous signal, and issued into a latch circuit 208.

Turning to the cited prior art, Muto discloses a subtractor 52 for calculating each of calculated phase differences and producing a difference signal representative of the calculated phase differences. The difference signal is then delivered to the comparator circuit 55, where the input comparator 57 detects an instance of coincidence of each calculated phase difference with the predetermined phase difference in the received signal (see, col. 11, lines 15-44). As such, Muto specifically discloses calculating the calculated phase differences, detecting the consecutive instances of coincidence, and knowing the presence of the particular signal sequence in the receive signal when the instances of coincidence reach a number substantially equal to the predetermined number N (see, col. 12, lines 30-32).

However, at a minimum, Muto does not disclose or suggest a digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form, as recited by claim 6. Muto merely discloses a subtractor 52 for subtracting a delayed and an undelayed signal outputted from the amplitude to phase processor 48, and a comparator circuit 55 for producing a coincidence signal representative of the consecutive instances of coincidence (see, col. 11, lines 7-44). Nowhere does Muto disclose or suggest a differential value of synchronous signals of reception packet data that is determined so as to detect a clock phase error of transmission data, a subtracting circuit for subtracting the N-th input from the N+1-th input of all reception data, or a segment synchronous signal, as recited by claim 6. The Office Action also does not address which elements of Muto correspond to the foregoing claimed elements. Thus, at a minimum, Muto fails to disclose or suggest the claimed elements as recited by the rejected claim.

Further, as recited by amended claim 6, only the phase errors of a second symbol and a third symbol of the segment synchronous signal are outputted as said clock phase error. In accordance with one embodiment of the present invention, when a particular signal sequence appearing at a periodic specified period is recognized to be a segment synchronous signal, the clock phase error of the segment synchronous signal is outputted. More specifically, as readily shown in Fig. 9 of Applicants' drawings, the signal "Sdet" is adjusted in time so as to latch the subtraction value at the timing after subtraction operation of the second and third segment synchronous signals of reception data by the latch circuit 205. In the latch circuit 208, by latching the signal "Segst" showing the

position of the segment synchronous signal, the clock phase error detecting circuit 105 outputs a clock phase error signal "Pherr." The signal "Segst" is also adjusted in time to the timing to be latched by the latch circuit 208, by the subtracted values of the second and third segment synchronous signals in the latch circuit 206 so that the four symbols of the segment synchronous signal can be detected.

However, nowhere does Muto disclose or suggest any segment synchronous signal, let alone suggest that the **second** symbol and the **third** symbol of the segment synchronous signal are outputted as the clock phase error. Indeed, Muto merely discloses that the output comparator 59 produces a result signal which indicates that the particular symbol pattern is found in a combination of the in-phase and the quadrature phase analog signals (see, col. 11, line 56 to col. 12, line 6). Thus, at a minimum, Muto fails to disclose or suggest that only the phase errors of a second symbol and a third symbol of the segment synchronous signal are outputted as said clock phase error, as recited by amended claim 6.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Muto fails to disclose the foregoing claim elements, it is clear that Muto does not anticipate claim 6.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF/AHC:jdj
Facsimile: (202) 756-8087
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